Abstracts

A Low-Current Linearity Sweet Spot in HFET's

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Planar doped HFET's exhibit a narrow bias region of low intermodulation distortion, a linearity sweet spot, at low drain current levels. The bias condition associated with this sweet spot is shown to be near the low-current inflection point of the transconductance versus gate voltage characteristic. It is also shown that the bias condition for the sweet spot can be controlled in dual-gate HFET's. This feature in the HFET characteristics can be exploited to design low-power front-end MMIC's with better intercept points for applications in wireless communications.

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